REMARKS

Claims 1-25 are pending in the present application. All of these claims were rejected in the present Office Action. By this amendment, Claims 19-22 and 25 have been amended to cure typographical errors and not for reasons related to patentability. Applicants respectfully traverse the rejections in light of the following remarks.

Claims 20-22 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite. The amendments to these claims herein are believed to address and resolve this rejection. Additionally, Claims 19 and 25 were rejected also under 35 U.S.C. §112, second paragraph, as being indefinite. The amendments to these claims are believed to address and resolve this rejection.

Claims 1-2, 4, 8-11, 20-22, and 24 were rejected under 35 U.S.C. §102(a) as being anticipated by Lawless et al. (U.S. Patent No. 5,818,469). Applicants respectfully traverse this rejection for the following reasons.

With respect to independent claim 1, the Office Action asserts that FIG. 1 and the accompanying text of Lawless disclose all of the elements of this claim. In particular, the Office Action equates the rendering threads 107 and 109 in FIG. 1 of Lawless as equivalent to the claimed reservation station. Additionally, the synchronizer thread 111 of Lawless is equated with the claimed "arbiter" and the hardware 115 of Lawless is equated with the claimed "command processing engine."

Assuming, for the sake of argument, these correlations made in the Office Action, Applicants respectfully submit that Lawless does not teach or suggest the claimed "command processing engine... that ... performs at least one processing command from the first command thread and thereupon updates the first command thread in the reservation station." In order to

meet this claimed element, Lawless would have to teach that the hardware 115, which is equated with the "command processing engine" would update a first command thread in either of the rendering threads 107 and 109, which are equated with the claimed "reservation station." This is simply not the case, however, as Lawless does not teach or suggest that the hardware 115 performs any updates of any of the threads within the graphics interface 103. Accordingly, Applicants respectfully submit that all of the elements of Claim 1 are not taught or suggested by Lawless.

With respect to independent Claims 2 and 4, Applicants respectfully submit that these claims are allowable on their merits and also due to their dependency on independent claim 1. Additionally, Applicants note that with respect to Claim 4, in particular, that Lawless does not teach or suggest that the command processing receives first and second command threads that are interleaved. Lawless merely teaches sequential ordering of a data stream, but does not teach or suggest interleaving of threads, which is a different concept than sequential ordering.

With respect to independent claim 8, this claim features "an arbiter coupled to the first reservation station and the second reservation station such that the arbiter retrieves a selected command thread from one of the plurality of command threads." Again, assuming the correlations made in the present Office Action of the featured "arbiter" to the disclosed synchronizer thread 111 of Lawless, Applicants submit that the above recited claim element of Claim 8 is not taught or suggested by Lawless. In particular, Claim 8 features the arbiter retrieving a selected command thread from one of the pluralities of command threads. In contrast, Lawless discloses that the synchronizer thread 111 (which is equated with the claim "arbiter") merely scans queue headers of the rendering threads for a next synchronization tag being delivered by the rendering threads 107 or 109, where the resultant data stream is

temporally ordered by the synchronizer thread 111 and sent to the graphics hardware 115 for rendering. It is noted that this teaching specifically does not disclose or suggest that the synchronizer 111 actually retrieves selected command threads from either of the rendering threads 107 or 109, but merely passively receives the threads. Accordingly, Applicants respectfully submit that Lawless does not teach or suggest this claim element and, thus, the rejection should be withdrawn accordingly.

With respect to dependent claims 9-11, these claims are submitted to be allowable on their merits and at least due to their dependency on independent claim 8, discussed above. Additionally, with respect to dependent claim 11, as discussed previously, Lawless does not disclose interleaving of first and second selected command threads, which is featured in this claim.

With respect to independent claim 20, this claim features "writing the selected command thread to a first reservation station at the selected command thread is one a plurality of first command threads and to a second reservation station if the selected command thread is one of plurality of second command threads." In contrast, Applicants submit that Lawless does not teach or suggest this claimed element. In particular, Lawless does not teach or suggest that thought to command threads are written to either of the rendering threads 107 or 109, which are equated with the claimed first and second reservation stations. Additionally, claim 20 features "retrieving a selected command thread from a plurality of command threads." The methodology disclosed in Lawless does not teach or suggest actually retrieving selected command threads, but merely receives or awaits rendering threads. Moreover, the Office Action had not specifically pointed to any disclosure in Lawless that actually teaches or suggests the features of claim 20.

Accordingly, Applicant respectfully submits that claim 20 is not anticipated by Lawless and the rejection should be withdrawn, accordingly.

With respect to dependent claims 21, 22, and 24, Applicants respectfully submit that these claims are allowable on their merits and also at least due to their dependency on independent claim 20.

Claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Lawless in view of Wyatt, et al. (U.S. Patent Application No. 2004/041814). Applicants respectfully traverse this rejection and submit that this claim is allowable on its merits and also at least due to its dependency on independent claim 1, discussed previously.

Claims 5-7, 12-19, 23 and 25 were rejected 35 U.S.C. § 103(a) as being unpatentable over Lawless in view of Airey, et al. (U.S. Patent No. 6,650,327). Applicants respectfully traverse this rejection for the following reasons.

First, with respect to dependent claims 5-7, 12-13 and 23, which depend from claims 1, 8, 20, respectively, these claims are submitted to be allowable on their merits and at least due to their dependencies. Accordingly, these claims are submitted to be allowable.

With respect to independent claim 14, the Office Action asserts that Lawless teaches all of the elements except for a first reservation station performing vertex operations and a second reservation station performing pixel operations, as well as an arithmetic logic unit (ALU) and a texture engine. Airey is alleged as teaching these elements and the Office Action asserts that it would have been obvious to combine the teachings of Airey with Lawless in order to "preserve precision of data in a frame buffer." Applicants respectfully traverse this rejection for the following reasons.

Applicants submit that the combination of Lawless and Airey do not teach or suggest all of the elements of claim 14. As apparently admitted in the present Office Action, Lawless does not teach or suggest the claimed elements of "arithmetic logic unit" or "texture engine operably coupled to [an] arbiter wherein the arbiter retrieves the first selected command thread from one of the plurality of pixel command threads and the plurality of vector command threads and the arbiter thereupon provides the first selected command thread to least one of the ALU and the texture engine." Additionally, Airey does not actually teach or suggest either of arithmetic logic unit or a texture engine coupled to an arbiter. Although, Airey might loosely disclose these types of units, the connections illustrated by Airey do not actually teach or suggest connecting such units to arbiter that, in turn, retrieves command threads, and provides the selected command threads to at least one of these devices. Rather, vertex data 131 and pixel data 132 is simply delivered directly to respective per-vortex operations and primitive assembly 135 and pixel operations 136. Furthermore, Lawless does not teach or suggest the claimed structure of claim 14. Accordingly, Applicants submit that the cited in references either combined or taken separately, do not teach or suggest all of the elements of claim 14 and the rejection should be withdrawn, accordingly.

Additionally, with respect to the stated motivation to combine, Applicants respectfully submit that it is unclear from the present Office Action or the teachings of the prior art how the combination of Airey and Lawless would result in preserving the precision of data in a frame buffer. Although Airey teaches the increase in the precision of data that can be stored in a frame buffer, by merely cobbling together Airey and Lawless, it is unclear how the teachings of Airey are beneficial when combined with Lawless. Furthermore, the intent of Lawless, which is the primary reference, is not directed to increasing or preserving precision of data in frame buffers,

but instead is directed to symmetric multi-processing of threads. The addition of floating point rasterization and floating point frame buffering taught by Airey does not necessarily further or help this intent of Lawless. Accordingly, Applicants submit that the stated motivation in the present Office Action does not make sense in light of the specific teachings of the cited references and is actually not a valid motivation.

With respect to dependent claims 15-19, these claims are submitted to be allowable on their merits and at least due to their ultimate dependency on independent claim 14, discussed above.

In light of the foregoing, Applicants submit that the present Application is in condition for allowance and request that the timely Notice of Allowance be issued in this case.

Respectfully submitted,

Date: June 22, 2005

By: _____
Patrick B. Law
Reg. No. 41,549

Vedder, Price, Kaufman & Kammholz, P.C.
222 N. LaSalle Street
Chicago, IL 60601
Telephone: (312) 609-7500
Facsimile: (312) 609-5005

CHICAGO/#1385831.1